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UNIT - II

8051 ARCHITECTURE

Introduction :-

- The first task faced when learning to use a new computer is to become familiar with the capability of the machine.
- The features of the computer are best learned by studing the internal hardware design, also called the architecture of the device to determine the type, number and size of registers and other circuitary
- The H/w is manipulated by accompayning set of program instructions or software.
- Once familiare with H/w & S/w, the system designer can then apply the microcontroller problem.

8051 Microcontroller Hardware :-

- 8051 µcontroller generic part number actualy includes a cohole family of µcontrollers that have numbers ranging from 8031 to 8751 and are available in N-channel Metal oxide Silicon (NMOS) and CMOS construction in a variety of package type.
- 8051, housed in a 40 pin DIP.

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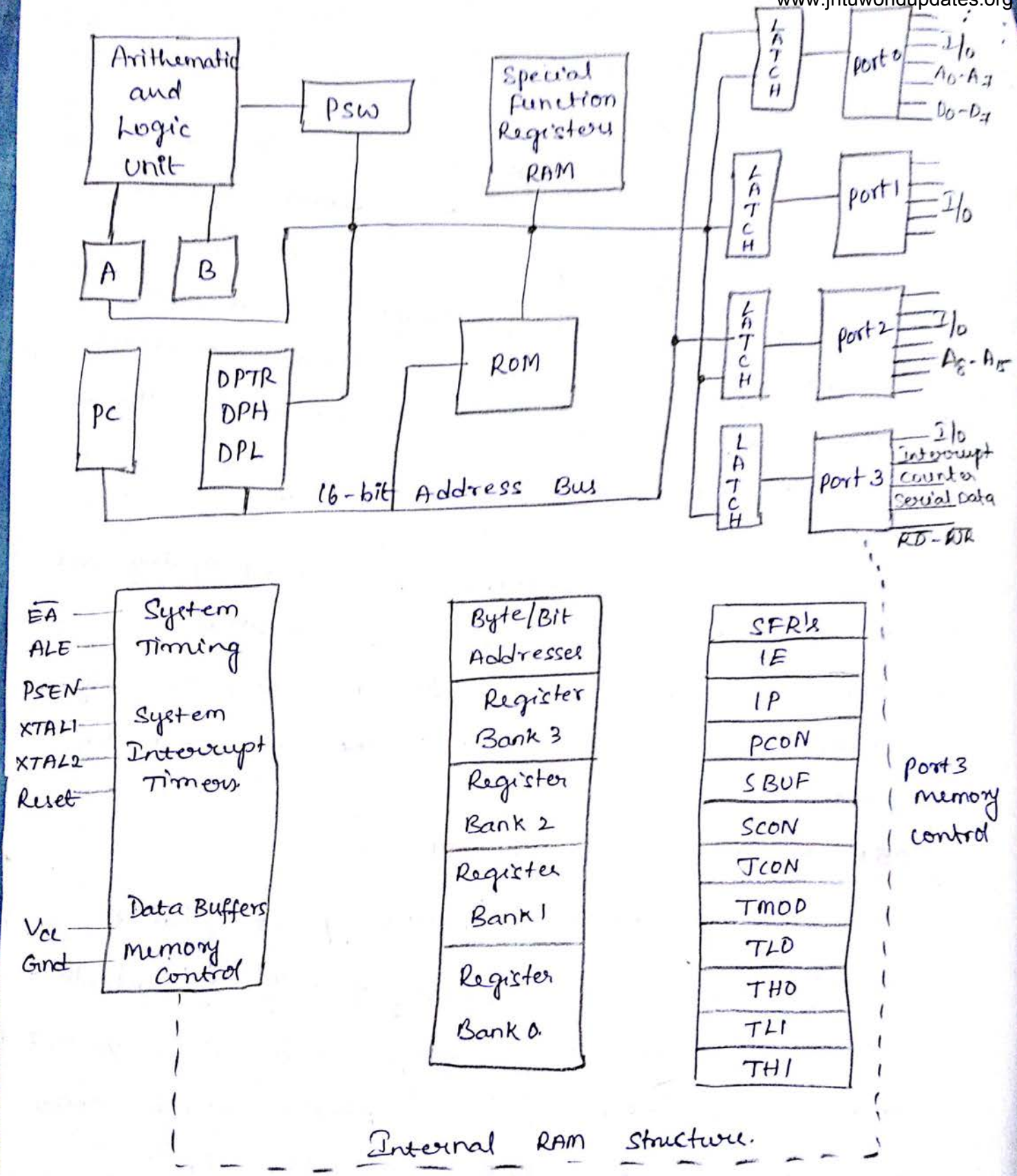
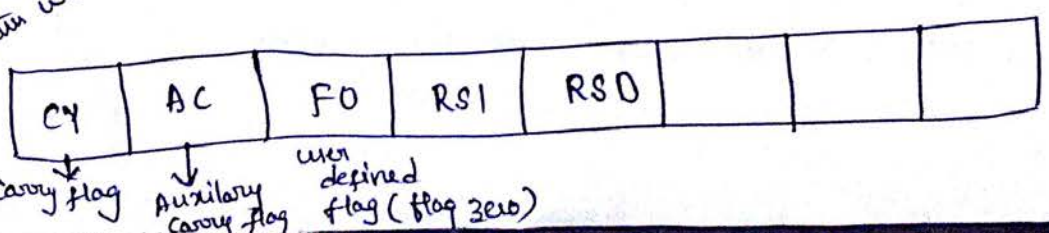


Fig : 8051 Block Diagram

PSW
Prog status word



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Microcontroller :- An integrated μp along with I/o ports and minimum memory into a chip (single chip - both RAM & ROM), parallel I/o, serial I/o, counter & clk circuit is called a μcontroller.

- The design of μctrller has the following advantages
  a) Built-in peripherals have smaller accen times hence speed is more.
  b) Hardware reduces to single chip microcomputer system
  c) Less Hardware, reduce PCB size and increases reliability of the system.

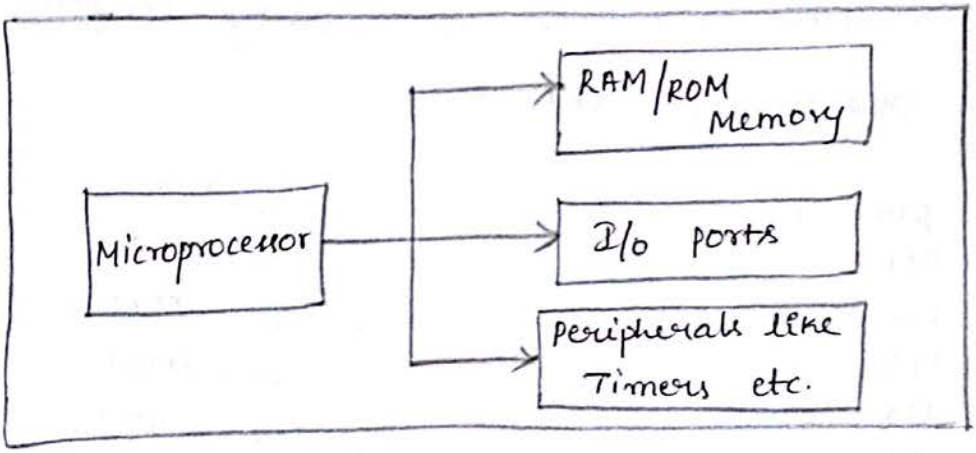

fig: Internal Block Diagram of μctrller

Overview of 8051 μctrller :-

The Before figure represent the architecture of 8051 μctrller whose overview is described below.

- Microcontroller contains most of the component required to form a μp system. It is called a single chip micro computer since it has the ability to easily implement simple control functions.
- The features of 8051 family are as follows :-
  1) 4096 Bytes (≈ 4KB) on chip program memory (ROM)
  2) 128 Bytes on chip data Memory (RAM)
  3) 4 Register Banks
  4) 128 bit addressable data memory (16 - bytes)

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5.) 64 KB's each program and external RAM addrenability.
6.) One μsec instruction cycle with 12 MHz crystal (11.052 MHz)
7.) 32 bidirectional I/o lines organized as four 8-bit ports.
8.) Multiple Mode, High speed programmable serial port.
9.) Two multiple mode, 16-bit Timers/counters
10.) Two level prioritized interrupt structure.
11.) Direct Byte and bit Addrenibility.
12.) Binary or decimal Arithematic.
13.) Integrated boolean processor for control applications.
14.) Signed-overflow detection & parity computation.

Pin-out (Pin Diagram of 8051)

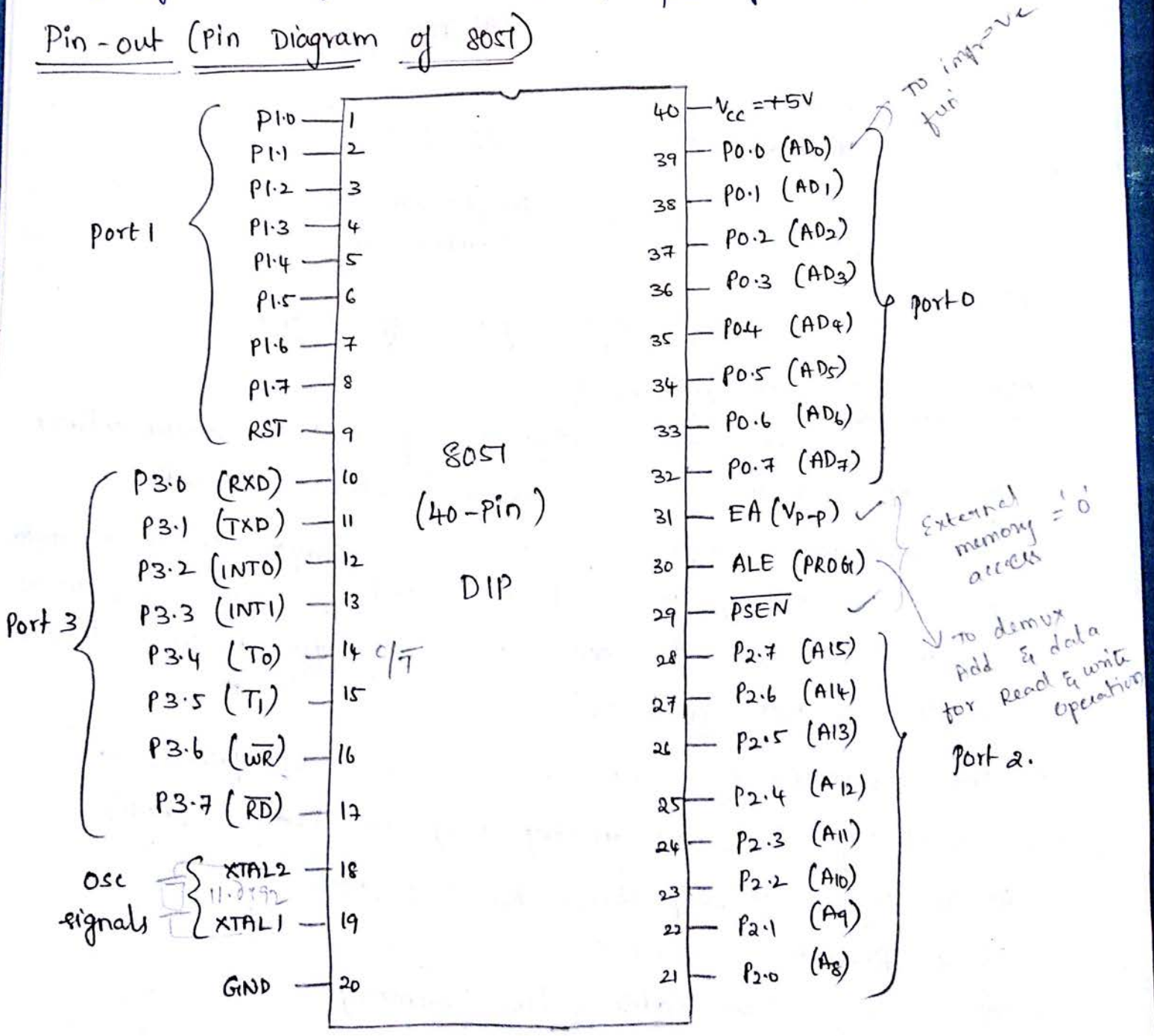

fig: 8051 pin diagram

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- The 8051 is packed in a 40-Pin DIP package that many pins of 8051 are used for more than one function.
- The 8051 has 32 I/o pins configured as four eight bit parallel ports (P0, P1, P2 & P3). All four ports are bidirectional i.e, each pin will be configured as i/p or o/p (or both.
- All port-pins are multiplexed except the pins of port-1. Each port consists of a latch, an o/p driver and and i/p buffer.

port 0 : (pins 32-39) :-

- port 0 pins can be used as I/o pins. The o/p drives and input buffers of port 0 are used to access external memory.
- port 0 outputs the low order bytes of the external memory address, time multiplexed with the data being written or read. Thus port 0 can be used as a multiplexed address/data bus.

port 1 : (pins 1-8) :-

port 1 pins can be used as only I/o pins.

port 2 : (pins 21-28) :-

- The output drives of port 2 are used to access external memory. port 2 o/p's the higher order byte of external memory address when the address is 16-bit wide.
- Otherwise port 2 is used as an I/o port.

port 3 : (pins 10-17) :-

All port pins of port 3 are multifunctional. They have special functions.

power supply pins V_{cc} (pin 40) and V_{ss} (pin 20) :-

-8051 operates on dc power supply of +5V w.r.to ground.

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Oscillator pins XTAL2 (pin 18) and XTAL1 (pin 19):-

For generating an internal clk signal, the external oscillator is connected at these two pins.

ALE (pin 30):-

AD_0 to AD_7 lines are multiplexed. To demultiplex these lines and for obtaining lower half of an address, an external latch and ALE signal of 8051 is used.

RST (Reset pin 9):-

It is used to reset 8051. for proper reset operation, reset signal must be held high atleast for two machine cycles while oscillator is running.

$\overline{PSEN}$ (program store enable : pin 29):-

- It is the active low output control signal used to activate the enable signal of the external ROM/EPROM. It is activated every six oscillators periods while reading the external memory. Thus this signal act as the read strobe to external program memory.

$\overline{EA}$ (External Access : pin 31):-

- when $\overline{EA}$ pin is high (connected to V_{cc}), program fetches to addresses 0000H to 0FFF H are directed to the internal ROM and program fetches to addresses 1000 H through FFFF H are directed to external ROM/EPROM.
- when $\overline{EA}$ is low (grounded), all addresses (0000H to FFFFH) are fetched by program are directed to the external ROM/EPROM.

CPU :-

- The CPU of 8051 Consists of 8-bit ALU with associated registers like A, B, PSW, SP, the 16-bit prog Counter (PC) and DPTR (data pointer) Registers. Along with these regs it has a set of SFR's.

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- 8051's ALU can perform Arithematic and logical functions on 8-bit variables.
- The Arithematic unit can perform +, −, *, /. Logic unit perform logical operations such as AND, OR, EX-OR, ROTATE, clear, complement.
- ALU also looks after branching decisions.

Note :— Unique feature of 8051 is that ALU can also manipulate one bit as well as 8-bit data types.
- Individual bit may be set, cleared, complemented, moved, tested and used in logic computation.

Internal RAM :—

- 8051 has 128-byte Internal RAM, which is organized as 3 distinct areas

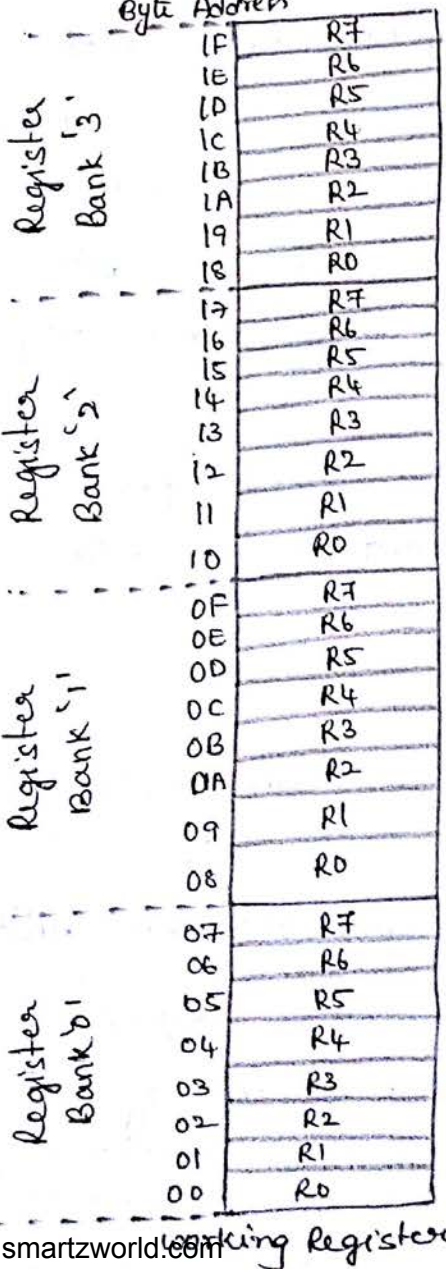
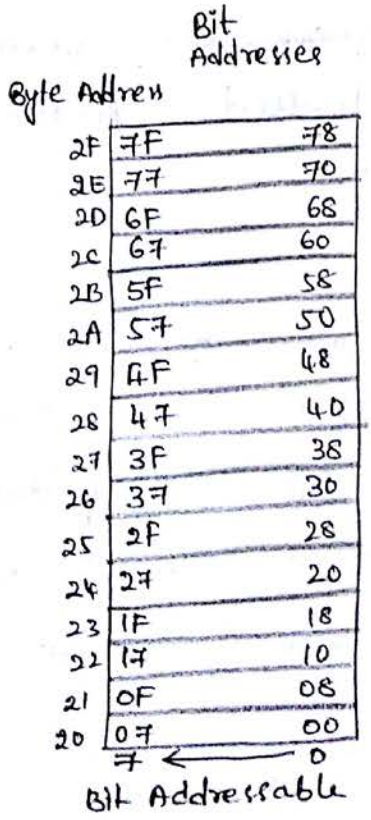
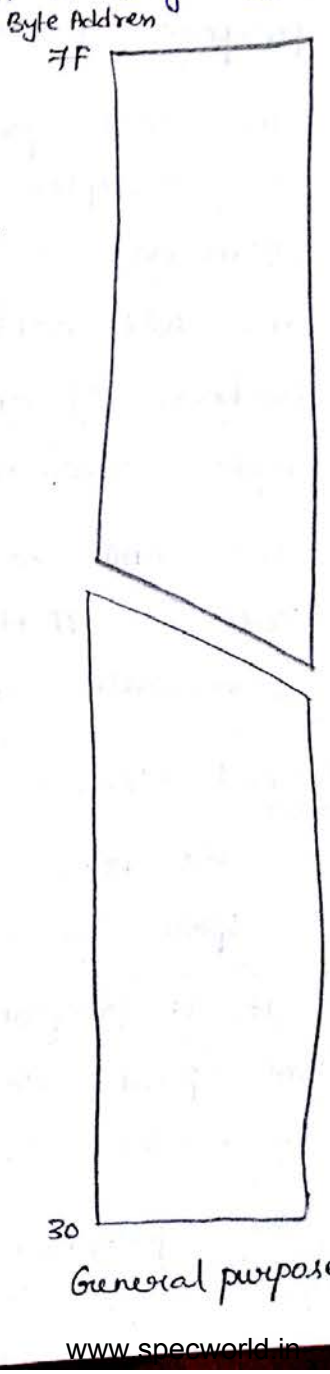


Fig : Internal RAM organization





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- The three distinct areas of RAM are
  ① * working Registers ② * Bit Addressable
  ③ * General purpose.

① - The first 32-bytes from addres 00H to 1FH of Internal RAM constitute 32 - working registers. They are org'zed in to four register banks that are numbered 0 to 3 and consist of 8-Regs each named R0 to R7.
- Each register can be addressed by name or by its RAM address. only one register bank is in use at a time.
- Bits RS_0 and RS_1 in PSW determine which bank of register is currently in use.
- Register Banks when not selected can be used as general purpose RAM. On Reset, Bank '0' is selected.

② - The 8051 provides 16 bytes of bit Addressable area.
- It occupies RAM byte addreses from 20H to 2FH, forming a total of 128 (16×8) addressable bits.
- An Addresable bit may be specified by its bit address of 00H to 7FH, or 8-bit may form any byte address from 20H to 2FH.

③ - The RAM area above bit addresable area from 30H to 7FH is called general purpose RAM. It is addrenable as byte.

Internal ROM :-

- The 8051 has 4KB of Internal ROM with addres span from 0000H to 0FFFH.
- It is programmed by manufacturer when the chip is built. This part can not be erased or altered after fabrication. This is used to store final version of the program.

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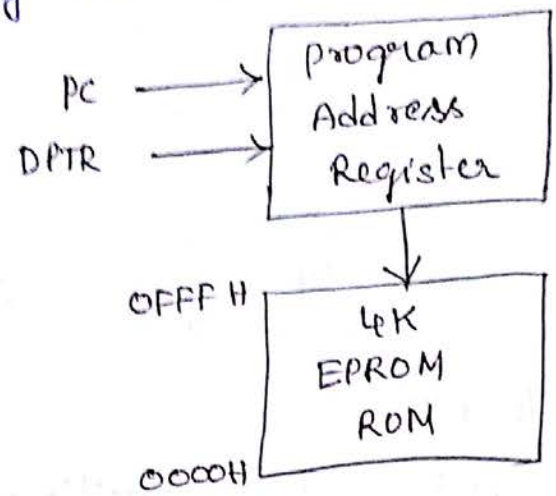
- It is accessed using program address registers the program addresses higher than OFFFH, which exceed the internal ROM capacity will cause the 8051 to automatically fetch code bytes from external prog. mem.
- However, code bytes can also be fetched exclusively from an external memory addresses 0000H to FFFFH, by connecting the external access pin (EA) to ground.



Input/output ports :-

- 8051 has 32 I/o pins configured as four 8-bit parallel ports (P0, P1, P2, P3)
- All 4 ports are bidirectional i.e each pin will be configured as i/p, o/p (or both) under s/w control.
- Each port consist of a latch, an output driver and an input buffer.
- The output driver of port 0 and port 2 and the i/p. buffers of port 0, are used to access external memory.
- port 0 outputs the low. order bytes of external memory address, time multiplexed with data being written or read, and port 2 outputs the high order byte of external memory address when address is 16-bit wide.
- otherwise port 2 gives the contents of SFR P2.

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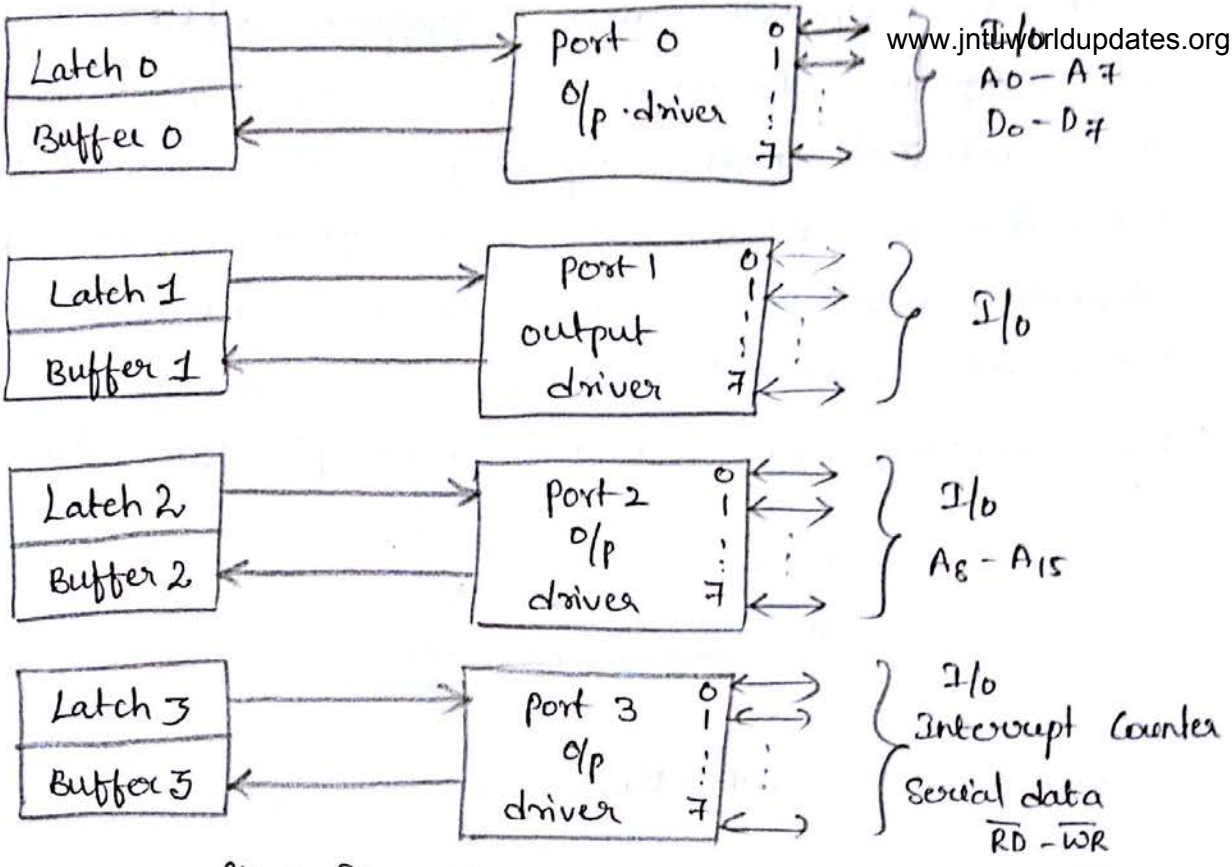

fig : I/O ports

— All port pins of port 3 are multifunctional. They have special functions including two external interrupt, two counter i/p's, two special data lines and two timing control strobes.

Symbol	Position	Name & Significance.
$\overline{RD}$	P3.7	Read data control output. Active low pulse generated by hardware when external data memory is read.
$\overline{WR}$	P3.6	write data control output. Active low pulse generated by hardware when external data memory is written.
T1	P3.5	Timer/counter 1 external i/p or test pin
T0	P3.4	Timer/counter 0 external input or test pin

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$\overline{INT1}$	P3.3	Interrupt 1 i/p pin. Low level or falling edge triggered.
$\overline{INT0}$	P3.2	Interrupt 0 i/p pin. Low level or falling edge triggered.
TXD	P3.1	Transmit data pin for serial port in UART mode. clock o/p in shift register mode.
RXD	P3.0	Receive data pin for serial port in UART mode. Data I/p pin in shift Register mode.

Register set of 8051 :—

Register A (Accumulator) :— It is an 8-bit register. It holds a source operand and receive the result of the arithematic instructions (+, −, *, /).

- The accumulator can be the source or destination for logical operations and no: of special data movements instructions, including look up tables and external RAM expansions
- Several functions apply exclusively to the accumulator: rotate, parity computation, testing for zero and soon.

Register B :— In addition to accumulator, an 8-bit B-Register is available as a general purpose reg when it is not being used for the hardware multiply / devide operations.

Program status word (Flag Register) PSW :— many instructions implicitly or explicitly affect several status flags, which are grouped together to form a

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$\overline{INT1}$	P3.3	Interrupt 1 i/p pin. Low level or falling edge triggered.
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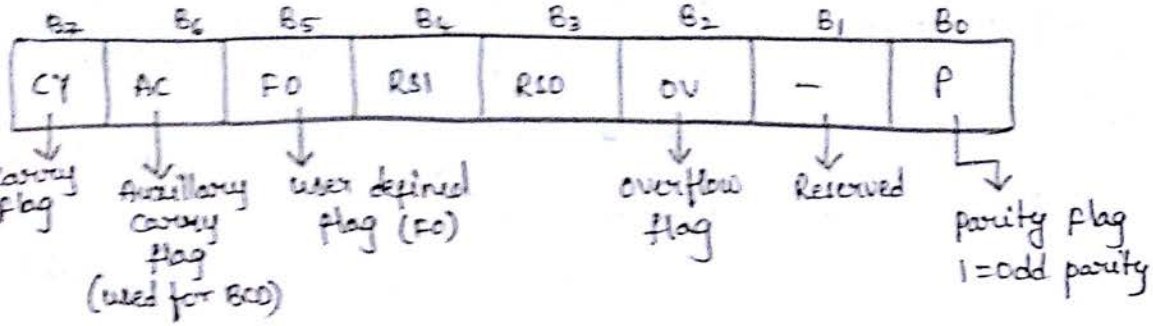
- program Status word.
- PSW is 8-bit word, containing the following information



Bit addressable as PSW.0 to PSW.7

- RS1, RS0 are used to select the working Register Bank.

RS1	RS0	Bank Selection
0	0	Select Register Bank 0 (00H - 07H)
0	1	Select Register Bank 1 (08H - 0FH)
1	0	Select Register Bank 2 (10H - 17H)
1	1	Select Register Bank 3 (18H - 1FH).

Stack and Stack Pointer :—

- The Stack refers to an internal RAM that is used in conjuction with Opcodes data to store and retrieve data quickly.
- SP reg is used by the 8051 to hold an internal RAM address that is called top of stack.
- SP is 8-bit wide. It is increased before data is stored during PUSH and CALL instructions and decremented after data is restored during POP & RET instructions.
- Thus stack array can reside anywhere in on Chip RAM. The SP is intialized to 07H after a reset.
- This causes the stack to begin at location 08H.

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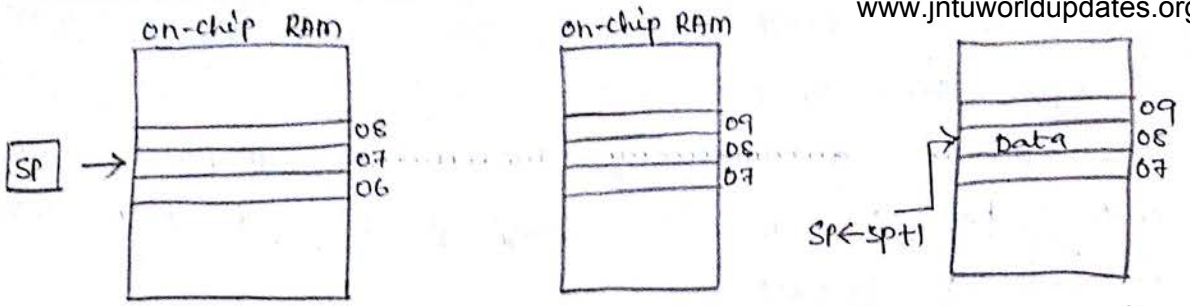
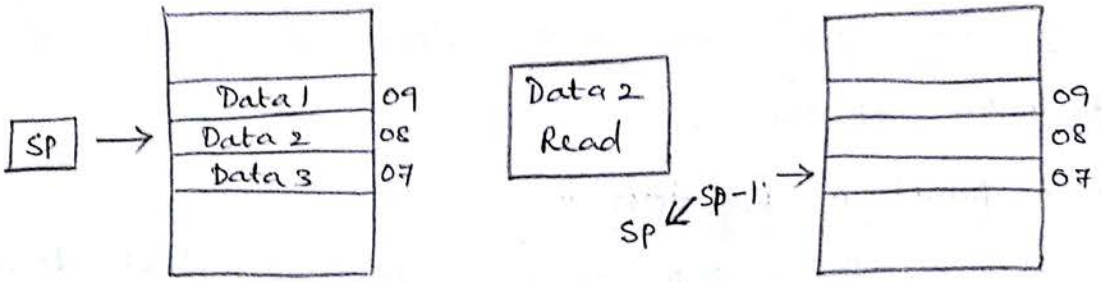


(a) status of stack and sp on Reset (b) store operation.

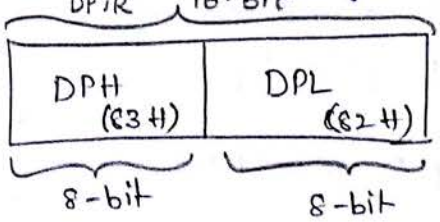


(c) Read operation.

Data pointer (DPTR) :—

The DPTR Register is made up of two 8-bit registers named DPH and DPL, which are used to furnish memory addresses for internal and external code access and external data access.

- DPTR serves as a base register in indirect jumps, look up table instructions and external data transfer.
- The DPTR does not have a single internal address, DPH and DPL are each assigned an address.



→ Memory accen.

Program Counter :—(PC) :—

- 8051 has a 16-bit PC. It is used to hold the address of memory location from which the next instruction is to be fetched.
- Due to this the width of the PC decides the maximum program length in bytes.

Stop bit (1).

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Eg: 8051 is 16-bit, hence it can address up to 2^{16} bytes (64K) of memory.

- The PC is automatically incremented to point the next instruction in the program sequence after execution of current instruction.
- It may also be altered by certain instructions. The PC is the only reg that does not have an internal address.

Special function Registers :-

The 8051 register operations that do not use the internal 128-byte RAM addresses from 00H to 7FH are done by a group of specific internal registers, each called a "special-function Register (SFR)" which may be addressed like internal RAM from 80H to FFH.

- Some SFR's are listed below.

	Name		function	Internal RAM address
1.	A	—	Accumulator	— E0
2.	B	—	Arithematic	— F0
3.	DPH	—	Addressing External memory	— 83 H
4.	DPL	—	" " "	— 82 H
5.	IE	—	Interrupt enable control	— A8
6.	IP	—	Interrupt priority	— B8
7.	P0	—	Input/output port latch	— 80
8.	P1	—		— 90
9.	P2	—		— A0
10.	P3	—		— B0
11.	PCON	—	power Control	— 87
12.	PSW	—	program status word	— D0
13.	SCON	—	serial port Control	— 98
14.	SBUF	—	serial port data Buffer	— 99
15.	SP	—	Stack pointer	— 81
16.	TMOD	—	Timer/counter mode ctrl	— 89
17.	TCON	—	Timer/counter Control	— 88

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Input/output pins, ports and Circuits :-

- The 8051 provides four ports for I/O Interfacing. Figure shows a functional diagram of a typical bit latch and I/O buffers in each of four ports.
- The bit latch is nothing but the one bit in the port SFR. It is represented as a D F/F.
- The signal "write to latch" acts as a clock input for D-FF.
- The data from the internal bus is clocked in response to a "write to latch" signal from the CPU.
- The $\bar{Q}$ o/p or Q o/p after inversion from D-FF is connected at the gate I/p of the driver FET.
- The ON and OFF state of the driver FET due to the data available at the o/p of latch decides the status of the o/p pin.
- It is possible to read the output of latch by activating "read latch" signal from the CPU. The actual port's status can be read by activating "read pin" signal.

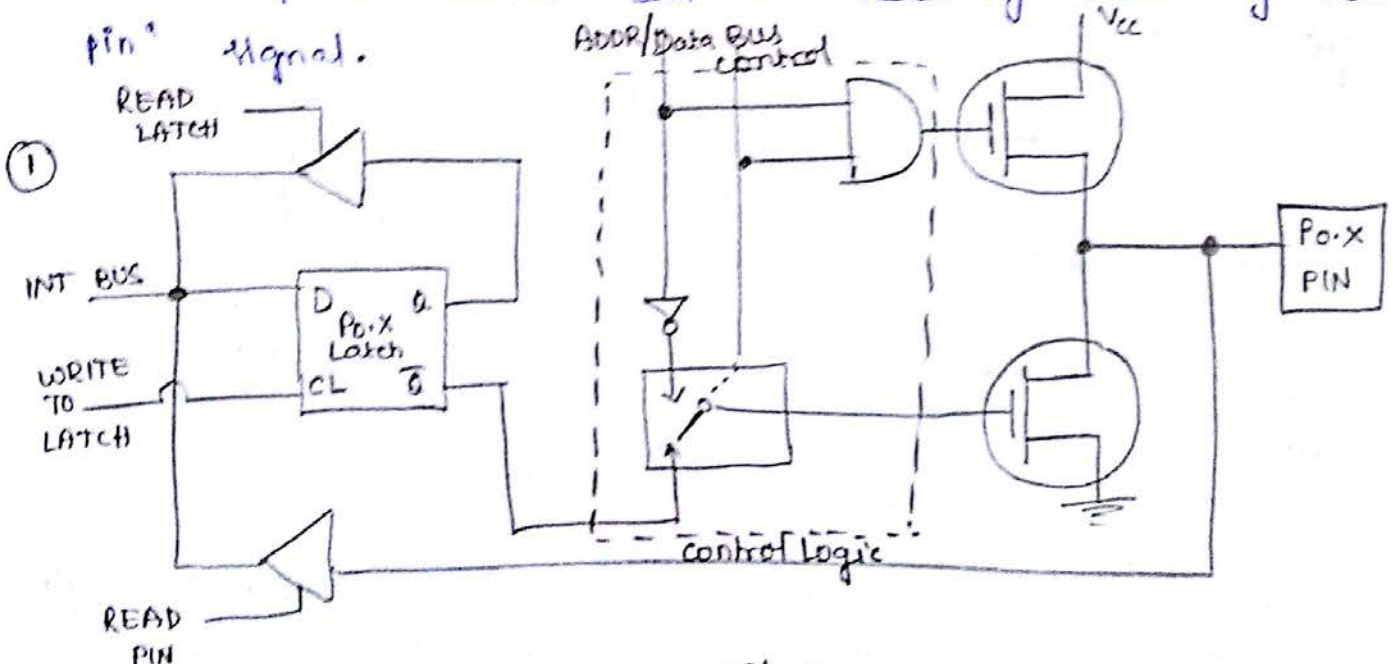

fig (a) : : port-0 bit :

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(2)

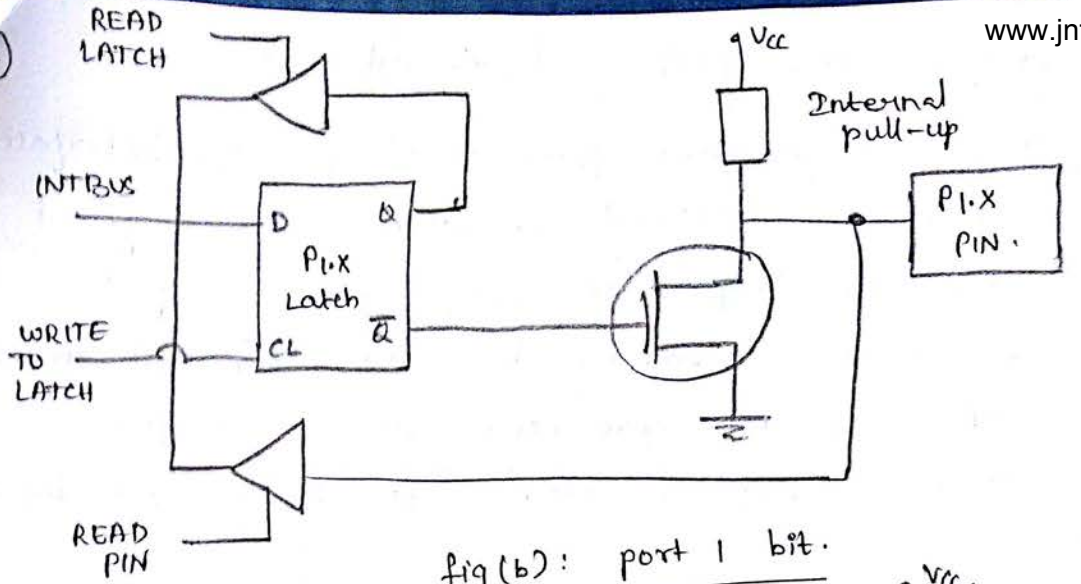

fig (b): port 1 bit.

(3)

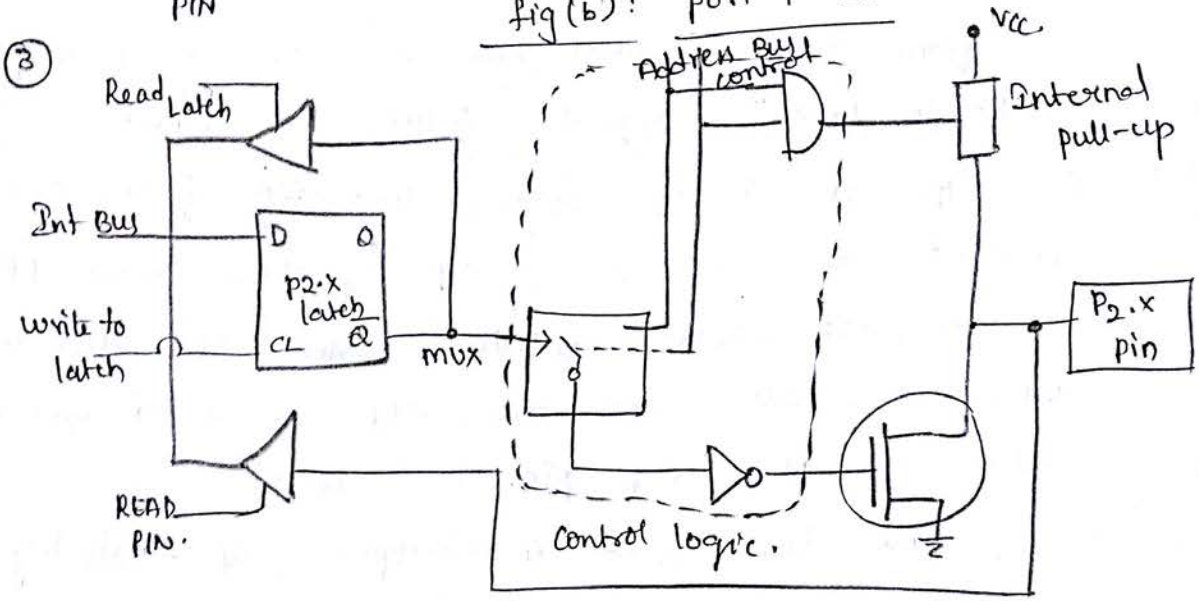

fig (c) : port 2 bit

(4)

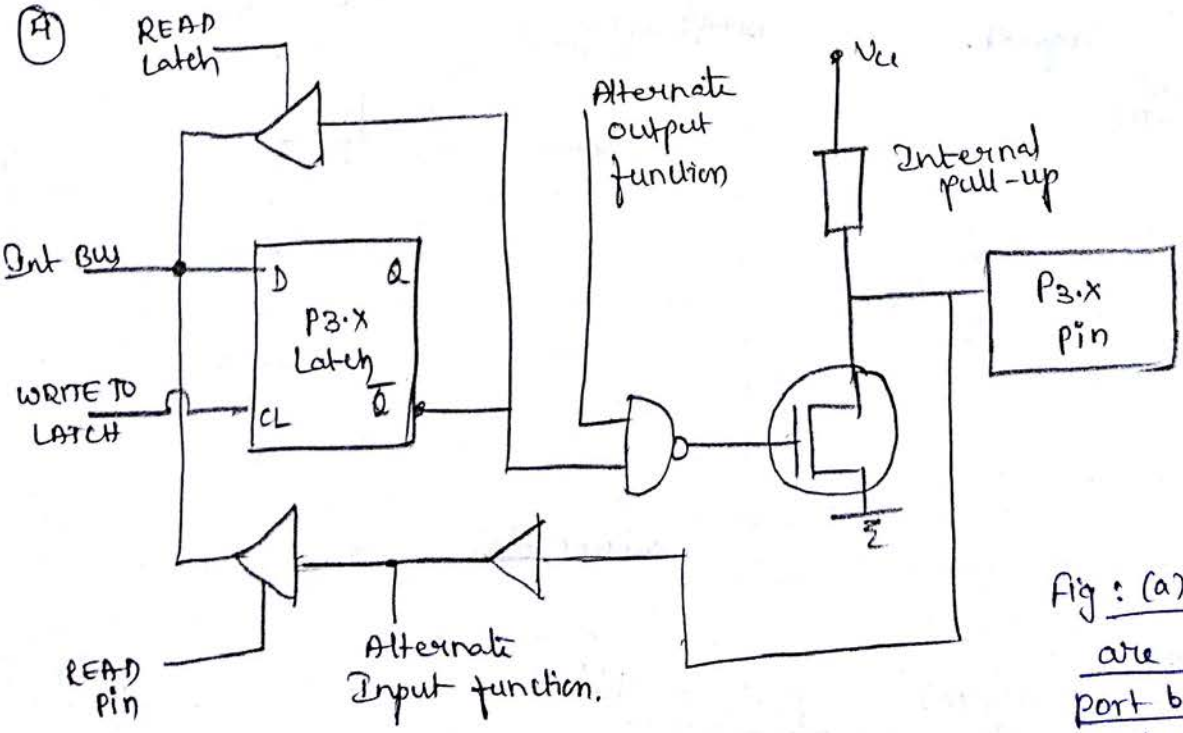

fig (d) : port-3 bit

fig : (a)(b)(d)(c) are 8051 port bit latches and I/o buffers

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- For port 0 and port 2 drivers are switchable to internal ADDR/DATA and ADDR bus resp, by internal CONTROL signal
- The switching is required to access external memory. During external memory accesses, the P2 SFR remains unchanged, but P0 SFR gets 1's written to it.
- port 3 has multifunction pins. Therefore, each pin of port 3 can be programmed to use as I/o or as one of the alternate function.

This is achevied by the another control input, "alternate output function".

- when latch bit of port 3 contains 1, the o/p level is controlled by control input, "alternate o/p function".
- the port pin can be configured as an input by writing 1 in the latch bit of the corresponding pin. It turns off the o/p driver FET.

Then for, ports 1, 2 & 3, the pin is pulled high by internal pull-up, but can be pulled low by an external source.

- There is no internal pull-up for port 0. Therefore, its output pin floats when 1 is written in the latch bit and pin can be used as a high impedence input.
- port 0 is said to be "true bidirectional", because when configured as an input it floats
- On the other hand the output of ports 1, 2 & 3 are pulled high with pull-up registers, when configured as an input. Thus they are sometimes called "quasi bidirectional" ports.

stop bit (1).

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Port	Functions
Port 0	* used as an I/o port * used as a bi-directional low-order address and data bus for external memory.
Port 1	* used as an Input/output port
port 2	* used as an Input/output port * used as a higher order address bus for external memory.
port 3	* used as Input/output port (or) used for alternate functions as shown below. P3.0 – RXD ; Serial data Input P3.1 – TXD ; Serial data output. P3.2 – $\overline{INT0}$; External Interrupt 0. P3.3 – $\overline{INT1}$; External Interrupt 1. P3.4 – T0 ; External Timer 0 Input. P3.5 – T1 ; External Timer1 Input. P3.6 – $\overline{WR}$; External memory write signal P3.7 – $\overline{RD}$; External memory Read signal

Timers and Counters of 8051 :–

– The 8051 has 2 timers, T0 & T1. They are independent of each other & can operate parallely

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Note :- The basic difference between time & counter is that for the basic timing timer uses clk frequency of chip while counter uses external freq.

Interval Timer :-

Timer is just hardware creating a delay, when started, it 'runs' and by the time it stops, a delay or interval has been created. Thus we call this an 'Interval Timer'.

Timer function :-

- A number is loaded in to timer register and timer is given the 'start' signal. The number in timer register keeps incrementing until it reaches max possible count. This is FF for 8-bit register and FFFF for 16-bit register.
- In one more step, the contents of reg rolls down to zero - this is the stop signal. The stop is indicated by the timer flag (TF).
- The rate at which timer reg increments is dependent - on clk signal of 8051. The higher the clk frequency, the faster the rate of increment of the timer registers.

Timer programming :-

Two timers - Timer 0 & Timer 1. Each timer has a timer Count reg which is 16-bit long. It is into this timer reg that we load the initial count. But only 8 bit can be

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timer 1 reg has TH1 & TL1

Timer Mode Register (TMOD) :-

TMOD is SFR at location 89H. This is used to define mode of operation of timer.

Gate	C/T	M1	M0	Gate	C/T	M1	M0
← Timer1 →				← Timer0 →			

Gate : Gate = 1 ; if starting of timer is done by H/w
= 0 ; if timer is enabled by S/w.

C/T : C/T = 1 ; Counter
C/T = 0 ; Timer.

M1, M0 :

M_1	M_0	
0	0	— Mode 0 ; 13-bit mode (seldom used)
0	1	— Mode 1 ; 16-bit mode
1	0	— Mode 2 ; 8-bit mode (with auto-reload)
1	1	— mode 3 ; Split timer modes.

Clock Source of the timer :-

When operating as an interval timer, the clk source is system clk itself. This frequency is ÷ by 12 for timer reg count to increment by 1.

Steps in programming interval timer :-

1. write MOD control word in TMOD.
2. write count in Timer register.
3. Start the timer
4. wait for overflow, and check the status of timer flag.
5. stop timer

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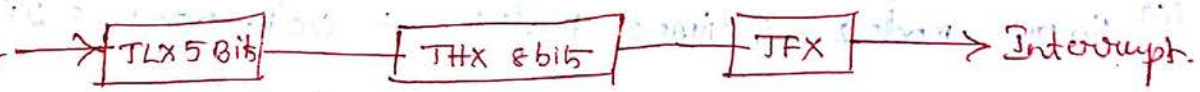
mode 0
THX as 8-bit counter
TLX as 5-bit counter
} 13 bit Timer/counter mode bits are set to 00B in TMOD.

mode 1
TLX is configured as full 8-bit counter
THX is like to mode '0'
} Mode bits are set as (01)B in TMOD

mode 2
uses TLX only as 8-bit counter
THX is used to hold a value loaded into TLX every time TLX overflows from FF H to 00 H.
} Mode bits set to '10' in TMOD.

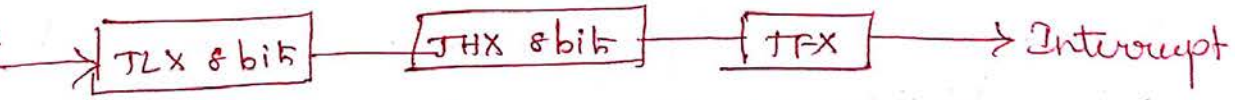
mode 3
Timer 1 in mode 3, causes it to stop counting.
Timer 0 in mode 3 becomes two Completely separate 8-bit counters
(TL0 Controlled by gate arrangement
TH0 Recive the timer clock under ctrl of TR1.)

(a)



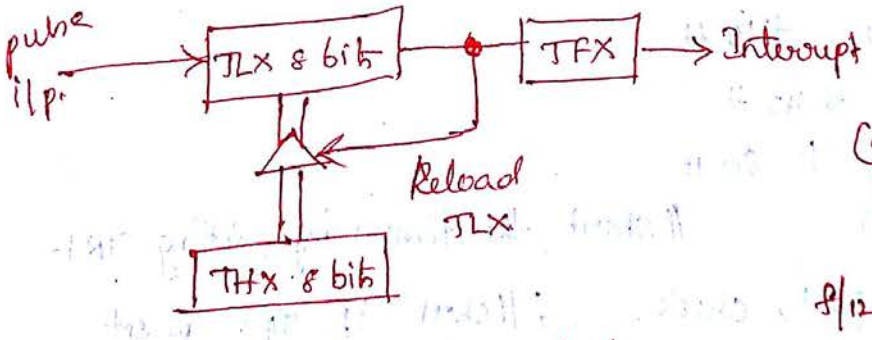
Timer Mode 0 : 13-bit Timer/counter.

(b)



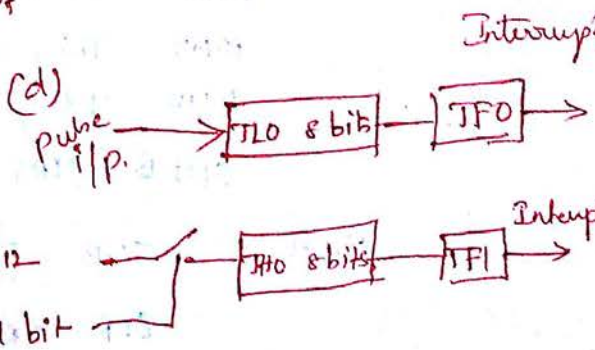
Timer mode 1 : 16-bit Timer/counter

(c)



Timer Mode 2 : Auto Reload of TL from TH

(d)



Timer mode 3 : Two 8-bit timers using Timer 0

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⇒ diff b/w timer & counter :—

" differ by source of the clock pulses to the counter

* when used as timer :— The clock pulse are source from oscillator through ÷12 ckt.

* when used as counter :— pin T0 (P3.4) supply pulses to Counter & pin T1 (P3.5) supply pulses to Counter and C/T bit in TMOD is set to 1

Eg : write mode ctrl words for following.

(a) timer1 Mode 1 → 0001 0000 = 10 H

(b) Timer0 mode 2 → 0000 0010 = 02 H.

(c) timer1 mode 2 & Time 0 mode 1 → 0010 0001 = 21 H

Program :-

use timer1 in mode1 to create a delay. Load 8042 H in timer reg. write a program for this also cal amount of delay.

Sol :-

```
        ORG 0
        MOV  TMOD, #10 H
        MOV  TL1, #42 H
        MOV  TH1, #80 H
        SETB TR1          // start the timer1 by setting TR1.
Check : JNB  TF1, check   ; // check if TF1 is set
        CLR  TR1
        END.
```

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writing the Mode control word :-

Consider time 0 in mode 1. For timer 0, only lower nibble of TMOD reg need to be used. upper nibble can be 0000. The lower nibble is 0001 for mode 1 usage. Thus mode control word is 0000 0001 i.e, 01.

Eg : write mode control words for the following :

(a) Timer 1 mode 1 → 0001 0000 = 10 H.

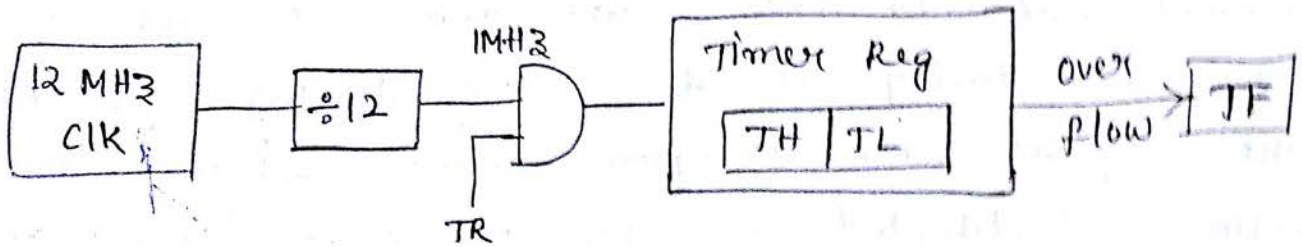
(b) Timer 0 mode 2 → 0000 0010 = 02 H.

(c) Timer 1 in mode 2 & Timer 0 in mode 1

→ 0010 0001 = 21 H.

Mode 1 programming :-

- In mode 1 the timer reg TH & TL are cascaded to get 16-bit reg in to which 16-bit number can be loaded.



Timer Control Register (TCON) :-

7	6	5	4	3	2	1	0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

- The TCON register has control bit and flags for the timers in the upper nibble and control bit and flags for the external interrupts in the lower nibble.

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timer to count.

TF0 : Timer 0 overflow

TR0 : Timer 0 Run control bit.

IE1 : External Interrupt 1. edge flag . set to 1 when high-to-low edge signal is received on port 3 pin 3.3.

IT1 : External interrupt 1. signal type control bit . set to 1 to enable external interrupt 1 to be triggered by a falling edge signal.

IE0 : External interrupt '0' edge flag.

IT0 : External interrupt '0' signal type control bit.

— This TCON SFR is bit addressed as TCON.0 to TCON.7.

Starting the Timer :-

This is done by s/w by setting start bit which is present in TCON Reg.

Detecting Timer overflow :-

Once the timer is started, the timer register increments, reaches the max and then rolls over to '0'. This corresponds to end of timing sequence.

— The flag set when overflow occurs. when timer overflow is detected we stop the timer (TR=0) and restart timing (TR=1) if we want to repeat the delay cycle.

Calculation of count required for delay :-

1. $N = T/t$ where T = Delay period.
   t = machine cycle period = $\left(\text{clkperiod}/12\right)$
2. Substract N from 65536
   i.e, 65536 − N.
3. The result of above in to Hex and store this

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Eg: Find the Count to be loaded in timer reg for using it in Mode1 with delay of 1.5msec when clk = 12MHz.

Sol: 1. $T = 1.5$ msec $= 1500$ μsec ;

$t = 1$ μsec

2. $N = T/t = \frac{1500\ \mu sec}{1\ \mu sec} = 1500$.

3. $65536 - N \Rightarrow 65536 - 1500 \Rightarrow 64036$

$\Rightarrow$ FA24 H

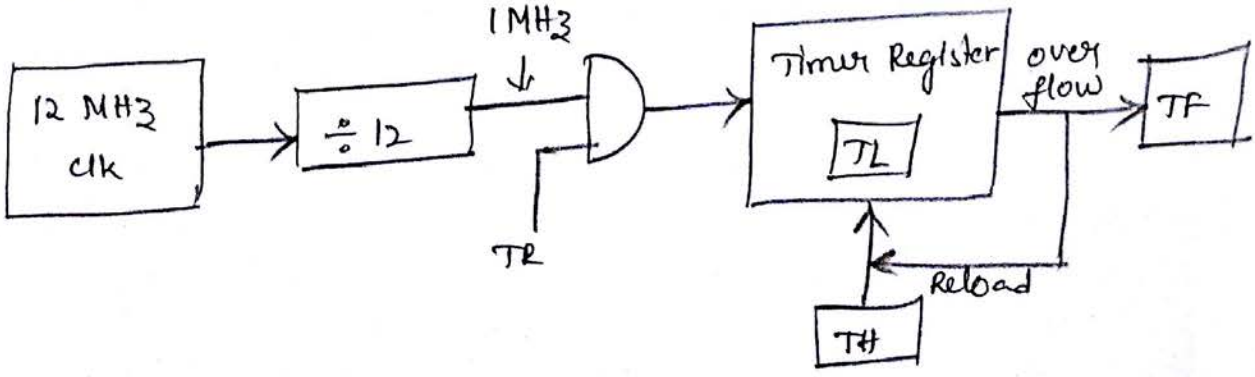
Mode 2 programming :-

- It is same as Mode 1 except for two aspects

(i) It is an 8-bit timer that it counts values from 0 to FF H.

(ii) Automatic Reloading is done.

- In this mode, count is to be loaded only into TH. 8051 copies it to TL Also.
- when timer is started, it is the TL which start incrementing upto FF and then rolls down to 0. The timer flag then gets set.
- For timer operation to continue, counter should be reloaded in to TL. This is done automatically as the procesor transfer the contents of TH to TL for a new delay to start.



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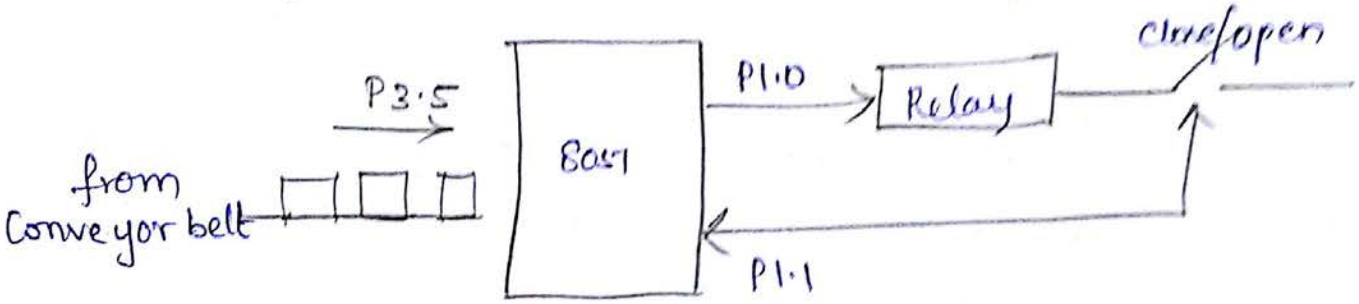
Counter programming :-

- The practical application of counting is that any action can be converted into a pulse.

Eg : objects on a conveyor belt can be counted

- In coming pulse train is fed into 8051 at P3.4 or P3.5 depending on which timer is to be used.

Eg: Counting 1000 events from conveyor belt



- There is unit which allows only 1000 items to be sent on conveyor belt.
- once 1000 items are got path is closed. then a waiting occurs until path is open again.
- P1.1 is controlling the path. It senses whether path is open or closed.
- program test P1.1 pin until it is set. the counting starts by inputting incoming pulse train on P3.5
- once 1000 event are Counted, timer flag is set and path is closed by Relay Controller.

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Eg: Find the count to be loaded in timer reg for using it in Mode 1 with delay of 1.5msec when clk = 12MHz. (12)

Sol: 1. $T = 1.5 \text{ msec} = 1500 \mu\text{sec}$;

2. $t = 1 \mu\text{sec}$

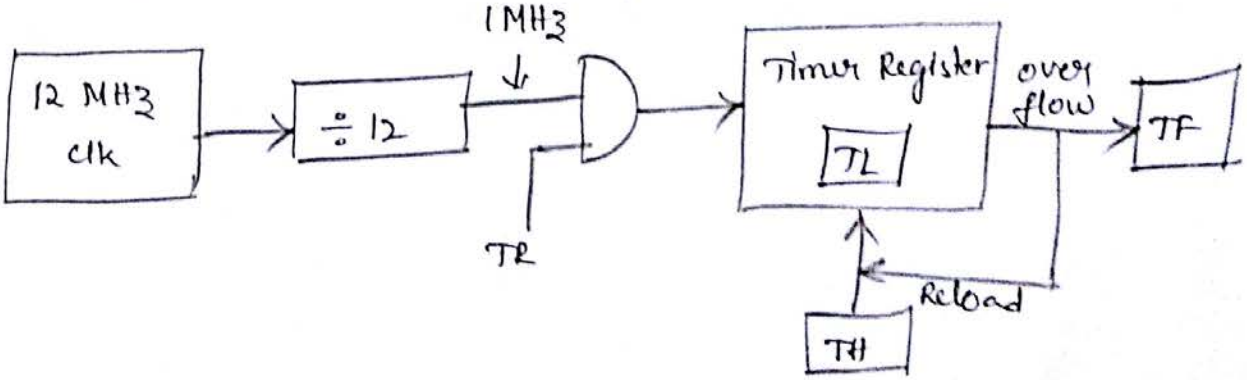
$N = T/t = \frac{1500 \mu\text{sec}}{1 \mu\text{sec}} = 1500$.

3. $65536 - N \Rightarrow 65536 - 1500 \Rightarrow 64036$

$\Rightarrow$ FA24 H

Mode 2 programming :-

- It is same as Mode 1 except for two aspects
  - (i) It is an 8-bit timer that it counts values from 0 to FF H.
  - (ii) Automatic Reloading is done.
- In this mode, count is to be loaded only into TH. 8051 copies it to TL also.
- when timer is started, it is the TL which start incrementing upto FF and then rolls down to 0. The timer flag then gets set.
- for timer operation to continue, counter should be reloaded in to TL. This is done automatically as the processor transfer the contents of TH to TL for a new delay to start.



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Interrupts of 8051 :-

Interrupt force the program to call a subroutine.

- Interrupt may be generated by internal chip operations or provided by external source
- An interrupt can cause the 8051 to perform a hardware call to an interrupt handling subroutine that is located at predetermined address in program memory.
- Six interrupt are provided by 8051, including "Reset". Three of these are generated automatically by internal operations and two of them are triggered by external signals provided by circuitary connected to pins $\overline{INT0}$ and $\overline{INT1}$

∴ The six interrupt are

→ Two external interrupt (EX0 & EX1); $\overline{INT0}$ & $\overline{INT1}$
→ Two timer interrupt for Timer 0 & Timer 1
→ one serial port interrupt (RI or TI)
→ Reset.

- All Interrupt functions are under the control of the prog.
- The programmer is able to alter control bit in the Interrupt Enable Register (IE), the Interrupt priority (IP) register and the Timer Control Register (TCON).
- After the interrupt has been handled by ISR, the interrupted program must resume operation at the inst where the interrupt took place.
- Program resumption is done by storing the interrupted PC Address on the stack in RAM.
- The PC Address will be restored from stack after an RETI instruction is excuted at the end of ISR.

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IE and IP function Registers :-

Interrupt Enable (IE) special func Register :-

7	6	5	4	3	2	1	0
EA	—	ET2	ES	ET1	EX1	ET0	EX0

Bit	Symbol	function.
7	EA	— Enable Interrupt bit. — cleared to '0' by program to disable all the interrupts.
6.	—	not implemented.
5	ET2	Reserved for future use.
4.	ES	Enable serial port interrupt. set to '1' by program to enable serial port Interrupt
3.	ET1	Enable Timer 1 overflow interrupt
2.	EX1	Enable external interrupt 1 . set to '1' by program to enable $\overline{INT1}$ Interrupt.
1.	ET0	Enable timer 0 overflow Interrupt.
0	EX0	Enable external interrupt '0'.

Bit addressable as IE.0 to IE.7

Interrupt priority (IP) Special function Register :-

7	6	5	4	3	2	1	0
—	—	PT2	PS	PT1	PX1	PT0	PX0

Bit	Symbol	function.
7	—	Not implemented
6	—	Not implemented
5	PT2	Reserved for future use.
4	PS	priority of Serial port Interrupt.
3.	PT1	Priority of Timer 1 overflow Interrupt
2.	PX1	priority of external Interrupt 1
1.	PT0	priority of Timer 0 overflow Interrupt

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PX0	0	priority of external interrupt 0.

Note: priority may be 1 (highest) or 0 (lowest)

Bit addressable as IP.0 to IP.7

Reset Interrupt :-

Reset is considered to be high priority interrupt because the program may not block the voltage on the RST pin. This type of interrupt is often called "Non-maskable".

- on Reset the program Jumps to addres 0000H.

Interrupt Enable / Disable :-

Bit in the IE Register are set to '1' if the corresponding interrupt source is to be enabled and set to '0' to disable the interrupt source.

- Bit 'EA' is a master, bit to enable or disable all of the interrupt.

Interrupt priority :-

- Bits set to '1' gives the interrupt a high priority & '0' assigns low priority.
- Interrupt with a high priority can interrupt a low low priority interrupt. the low priority interrupt continues after the higher is finished.
- If two interrupt with same priority occur at same time, then they have the following ranking.

1. Reset
2. IE0
3. TF0
4. IE1
5. TF1
6. Serial = RI or TI.

for eg: the serial interrupt could be given the highest priority by setting the PS bit in IP to '1' and all others to '0'

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Interrupt Destinations :-

Each Interrupt source causes the program to do a hardware call to one of the dedicated addresses in program memory.

- All the interrupt are vectored interrupts and the destinations are given as

Interrupt	Address (Hex)	Pin
Reset	0000	9
IE0 (EX0)	0003	12 (P3.2)
TF0	000B	.....
IE1 (EX1)	0013.	13 (P3.3)
TF1	001B.	.....
SERIAL	0023	.....

Serial Communication / Serial Data Input/Output :-

One cost effective way to communicate between computers is to send and receive data bit serially.

- The 8051 has a serial data comm'tion circuit that uses register SBUF to hold data.
- Register SCON controls data. Communication, register PCON controls data rates, and pins RXD (P3.0) and TXD (P3.1) connect to the serial data network.
- SBUF is physically two registers. One is write only and is used to hold data to be transmitted out of the 8051 via TXD. The other is read only and holds received data from external sources via RXD. Both registers use address "99H".

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— There are 4 programmable modes for serial data Comm' that are choosen by setting the SMx bit in SCON

SCON (Serial Port Control) special function Register :—

7	6	5	4	3	2	1	0
SM0	SM1	SM2	REN	TB8	RB8	TI	RI

Bit	Symbol	function.
7.	SM0	Serial port mode bit 0. set/cleared by program to select mode.
6.	SM1	Serial port mode bit 1. set/cleared to select mode

SM0	SM1	Mode	Description
0	0	0	— shift register ; baud = $f/12$
0	1	1	— 8 bit UART ; baud = Variable
1	0	2	— 9 bit UART ; baud = $f/32$ or $f/64$
1	1	3	— 9 bit UART ; baud = Variable.

5.	SM2	Multiprocenor Communications bit. set/cleared by program to enable multiprocenor Communications in modes 2 and 3.
4.	REN	Receive enable bit. set to 1 to enable reception; cleared to '0' to disable reception.
3.	TB8	Transmitted bit 8. set/cleared by prog' in modes 2 & 3
2.	RB8	Received bit 8. Bit 8 of received data in modes 2 & 3
1.	TI	Transmit interrupt flag. set to '1' at the end of bit 7 time in mode 0, and at the beginning of the stop bit for other modes.
0.	RI	Receive interrupt flag. set to '1' at the end of bit 7 time in mode 0, and halfway through the stop bit for other modes.

Bit Addresables as SCON.0 to SCON.7.

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PCON Special function Register :- (power control register).

7	6	5	4	3	2	1	0
SMOD	-	-	-	GIF1	GIF0	PD	IDL

Bit	Symbol	function
7	SMOD	Serial baud rate modify bit. It is 0 at reset. It is set to '1' by the program to double the baud rate.
6, 5, 4		not defined
3	GIF1	General purpose user flag bit 1. set/ cleared by program
2	GIF0	General purpose user flag bit 0.
1	PD (shutdown)	Power down bit. It is set to '1' by prog' to enter power down configuration of µcontroller.
0	IDL (sleep)	Idle mode bit. It is set to '1' by prog' to enter idle mode Configuration of µcontroller.

* PCON Register is not bit addressable.

Operating Modes of Serial port :-

⟹ RXD
TXD ⇒ clk.

Mode 0 :-

This mode is also called as "shift Register data transmission" mode.

- For this mode, the SM0 and SM1 bit of SBUF register must be set to 00B.
- In this mode, Serial data enters and exits through RXD.
- The TXD serves as clock.
- 8 bit are transmitted/received : 8 data bits (LSB first)

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- In mode '0' the baud rate is fixed at 1/12 the oscillator frequency.

$$\text{Baud rate} = \frac{\text{Frequency of oscillator}}{12}$$

- The serial port in mode 0 is an example of Synchronous communication.
- The baud rate in mode 0 is much higher than standard communication rates.

transmit → TXD
Receive → RXD

Mode 1 :-

In this mode, 10-bit are transmitted (through TXD) and received through (RXD) :

A start bit (0), 8 data bit (LSB first), and a stop bit (1).

- on receive, the stop bit goes into RB8 in special fun Reg SCON.
- In this mode the baud rate is variable
- This mode is also referred to as "standard UART"
- It it an 8-bit UART, Eg of Asyn comm'
- ∵ it is asyn, Clk is not required to send data
- SBUF (Serial port Buffer) reg acts as full-Duplex receiver/transmitter by setting SM0 & SM1 to 01 B.
- As soon as 10-bit are sent, the Interrupt flag (TI) is set, signalling that entire byte has been transmitted.

Mode 2 :-

This mode is also referred to as "Multiprocessor mode".

- In this mode, 11-bit are transmitted instead of 10-bit
- 11 bit are : a start bit (0), 9 data bits & one stop bit (1).

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i.e, a start bit (0), 8 data bits (LSB first), a programmable 9th data bit and a stop bit (1).

- During transmission, 9th bit is copied from the TB8 of SCON register and while receiving the 9th bit is stored in the RB8 bit of SCON reg and stop bit is ignored.
- The baud rate is programmable to either 1/32 or 1/64 of oscillator frequency.

∴ Baud rate $= \frac{2^{SMOD}}{64} \times$ freq of oscillator.

Mode 3 :—

In this mode, 11-bits are transmitted (through TXD) or received (through RXD) : a start bit (0), 8 data bits (LSB first), a programmable 9th data bit and stopbit (1).

- In fact, mode 3 is similar to Mode 2 in all respects exept the baud rate.

The baud rate is variable in Mode 3.

Mode	Transmission Format	Baud rate.
0	8 - data bits	$\frac{1}{12}$ Oscillator frequency.
1	10-bit (start bit + 8 data bits + stop bit)	Variable.
2	11-bit (start bit + 8 data bits + programmable 9th data bit + stop bit)	programmable to either 1/32 or 1/64 of oscillator freq.
3	11-bits (start bit + 8 data bits + programmable 9th data bit + stop bit)	Variable

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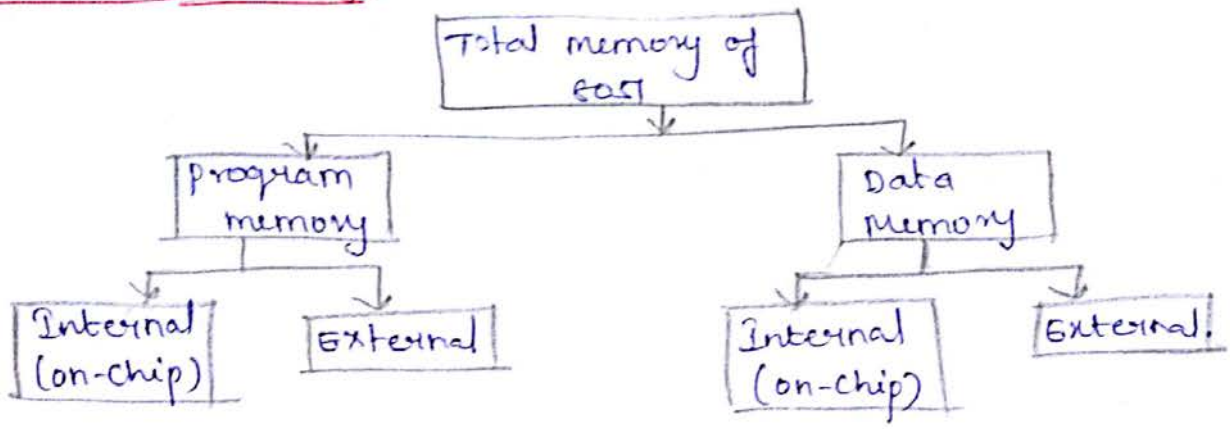
External Memory :-



- In 8051, when the $\overline{EA}$ pin is connected to V_{cc} ($\overline{EA}=1$) it indicates that the program code is stored in the microllers on-chip (Internal) memory.
- when the $\overline{EA}$ pin is grounded ($\overline{EA}=0$) then it indicates that program code is stored in External memory.
* The memory space on the 8051 chip is not constrained with the internal RAM and ROM.
- There are various pins which can be used to enable external RAM & ROM chips.

Need for Adding External Memory :-

① As money and time are two important, when it reaches the prototype stage, trail and error method cannot be applied to modify the contents of ROM. Thus 8751 version of EPROM with 4K volatile memory can be used to program & erase as needed.

- Addition of 8751 does not make much difference to the layout of 8051, but there are few drawbacks.
  * The size of program code is limited to 4096 Bytes
  * Skilled EPROM programmers are required, in order to program the non-standard 40 pin port.

(2.) The size-related limitation (4096 bytes of prog. code) in 8751 can be overcome by using ROM less 8031. The size of the program can be made upto 64K in order to serve high-level lang. progs having more than 4K program size.

To do so, a pin named $\overline{EA}$ (External Access) of 8031 is grounded which results in the transfer of the program code in to External EPROM.

(3.) when internal data storage of 128-bytes donot suffice the size of the program; use external RAM memory of upto 64K through DPTR.

The connection b/w 8031 & external mem is shown in TB.

- The external ROM can be accessed by grounding $\overline{EA}$ pin. It can also be accessed when the address contained in PC is greater than OFFFH.

Hence both Internal & External ROM can be automatically used by 8051.

---

max 8051 ROM is
= 4K
(i.e, 000H to FFFH

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